Solutions to Today's Low Voltage Power Design Challenges Using High-Efficiency, Non-Isolated Point of Load Converters
A Discussion of the Interpoint™ MFP Series™ Point of Load Converter

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1 Abstract

Design engineers face numerous challenges satisfying the power delivery requirements of today's electronic systems. The multitude of low-voltage, high current loads and increased system power efficiency requirements make yesterday's typical design approaches increasingly less practical, and design requirements increasingly more difficult to achieve. This paper presents a discussion of these challenges and previous common solutions and introduces the Point of Load (POL) converter as an ideal high-efficiency, high-reliability solution.

POL converter implementation is discussed and relevant issues highlighted, including main power input bus considerations, conducted noise, control stability, current limiting and current sharing, environmental ruggedness, design analysis and some of the many features offered in top-of-the-line POL converters. Product usability, the ability of the end user to successfully implement the POL and attain the specified performance specifications over the full environmental and electrical specifications without additional circuitry, is discussed. The Interpoint MFP Series™ POL is presented throughout the paper and how it addresses many of the design challenges presented is discussed. While the authors clearly favor a particular solution, this discussion is intended to be of general use to all engineers tasked with powering low-voltage loads in high-reliability systems.

2 Intermediate Bus Architectures Using Point of Load Conversion

System designers are faced with many challenges when providing low voltage DC power in distributed power architectures. System bus power is delivered at a much higher bus voltage in order to reduce weight and resistive power loss as this DC power is delivered extended distances from the source. System source voltages are commonly a nominal 12V, 28V, 48V, 120V and in some cases 270V.

These bus voltages are unique to differing platforms and can vary in regulation from +/- 10% to as much as +/-50% of the nominal value. These voltages must be stepped down and tightly regulated at the point of use due to the low voltages required as precision inputs for today's electronics. Low-voltage load requirements typically range from 0.8V to 3.3V and are continuing to drop as Moore's Law [3] and associated increases in semiconductor logic density make faster computing possible. The output current demand to power such loads continues to increase as the numbers of gates and clocking frequencies increase.

The down-conversion of voltage may occur in one, two, or three steps. As an example, an unregulated 28V bus voltage may be distributed throughout a system. This bus may be stepped down to 12V or to 5V at the circuit card level while the final step down to the lowest desired voltage may occur as close as practical to the load. Although power is lost at each conversion step, it is not practical to deliver the lowest voltages over significant distances due to the high currents and consequent high resistive losses which would be incurred. Designers must weigh the advantages and disadvantages of multi-stage power conversion, the tradeoffs of distance, and the need for intermediate voltages to power other circuit elements that often drive the architecture.

A common requirement in many applications is the need for the final down-conversion to occur as close to the load as possible. This conversion is often performed by a Point of Load (POL) converter. Proximity to low-voltage digital loads such as FPGAs, ASICs, and DSP processors is critical. These loads are capable of inducing large load transients with rapid load changes while requiring tight voltage regulation coupled with high DC currents. Close proximity reduces the parasitic inductances and associated line voltage excursions that can result from load transitions.

Power conversion is typically accomplished in multiple stages to reach the final load voltage. Isolation and regulation are two key requirements and may be implemented at different stages depending on system architecture. POL devices on the market today are most commonly offered as 5V or 12V input converters and less commonly as 3.3V inputs. The first stage converter upstream from the POL often includes system isolation from the input to output grounds, a common system requirement. The POL, to maximize efficiency and power density, is almost never isolated.

The first conversion stage may be tightly regulated or not regulated at all, depending on the regulation of the source and the acceptable input range of the POL. A tightly regulated system source would favor the selection of a loosely regulated bus converter. While the choice to use a first-stage converter that is not regulated can greatly improve the efficiency of the converter, the associated variation of bus voltage will be much higher. An unregulated bus converter output will vary in direct proportion to the input voltage. Ranges of +/-20% or more are common and depend on bus specifications. A POL able to accept a wide input voltage range offers flexibility in efficiency optimization to the user.

The choice of an intermediate voltage, 3.3V, 5V or 12V, depends on several factors: available product, distance of the bus converter from point of use, and whether or not the intermediate voltage is required elsewhere in the system. The usage of the intermediate voltage by digital devices is one reason that a 5V or 3.3V bus is often tightly regulated. A 12V intermediate bus is often loosely regulated because it typically powers less sensitive analog loads. Figure 1 illustrates an intermediate bus architecture with an isolated DC to DC bus converter stepping down a distributed bus voltage Vbus to an intermediate voltage V1 which is used to power multiple POL converters. The POLs are then used to power the loads at differing voltages V2, V3 and V4.

It is important to note when considering system level performance that the POL converter efficiency should not be considered by itself. Different POL converters require different levels of intermediate bus regulation and the more stringent the POL input requirement the less efficient the intermediate stage will typically perform. Stage conversion losses and interconnect losses between stages need to be included when calculating overall system efficiency.
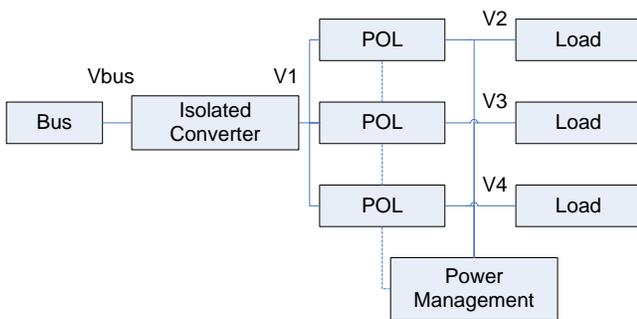
Figure 1: Typical intermediate bus architecture

3   Interpoint MFP Series™ Converters

Crane Aerospace & Electronics has recently launched the first in a family of non-isolated POL converters. The MFP includes many of the features requested and addresses the challenges reported by thousands of customers. Common challenges facing the power system designer along with the way in which they are addressed by Interpoint products are discussed in this paper.

The MFP is a high-reliability, high-efficiency POL converter designed for use with a 3.3V or 5V input bus, with under voltage shutdown below 3V and overvoltage shutdown above 6V to protect the system. The MFP includes five precision output voltage set-points of 0.64V, 0.8V, 1.6V, 2.5V, or 3.3V. The output voltage can be digitally selected while values between the digital set points can be established with a single trim resistor. The product is available in a range of screening options including the standard temperature range of -55C to 125C, extended temperature of -70C to 150C, radiation hardened models up to 100KRad(Si), and available compliance screening to Class H or Class K of MIL-PRF-38534 [1]. Some of the additional features include synchronization, current share operation, power-up sequencing, all-inclusive input and output filtering, and an internal solid state power switch all contained within a small, hermetically sealed package.

4   Electrical Design Considerations

4.1   Input Voltage Range

The input voltage range of a POL device sets the regulation requirements of the upstream power source. A narrow input range requires a tightly regulated supply and has little tolerance for line drop and temperature variation. In such situations, the POL input may require additional protection to avoid damage. A wide input range

allows a more loosely regulated and often more efficient source and tolerates variations in input voltage and temperature.

When operating over a wide input range, the difficulty in low input voltage operation is providing adequate voltage for full enhancement of the internal synchronous MOSFETs. This is one of the reasons many POL converters do not operate below an input of 4.5V. Very low input voltages often require the use of a higher voltage external supply to power the internal circuitry of the POL. If required, the designer must consider the additional power demands, cost, and board space associated with an external supply. Additional complications may result if the external supply must be active prior to power-up of the POL or during shutdown of the POL.

The MFP has a wide input range of 3V to 6V to enable operation with either a 3.3V or 5V bus voltage. The wide input range also means that the MFP is tolerant of loosely regulated buses of -40% to +20% for 5V inputs and -10% to +80% for 3.3V inputs.

The ability of the MFP to operate with such low input voltages without an external supply is possible because of a unique internal housekeeping power supply which begins providing an internal 8V rail at an input of only 2V. This well-regulated internal supply is more than adequate for low conduction loss switching and allows for proper operation of the under voltage lockout and input Solid State Switch (SSS) circuitry.

4.1.1 Input Bus Voltage Transients
Important to system reliability is the ability to prevent the propagation of source faults to the load. A failure of the first stage converter regulation that results in an open loop condition or in excessive output voltage could easily damage many POLs that have limited maximum input voltages.

The MFP is unique in that it contains a patent pending series SSS circuit at the input to the POL, as shown in Figure 2. This switch will open whenever the input voltage becomes excessive, providing protection for input transients of up to 15V, preventing damage to the POL.
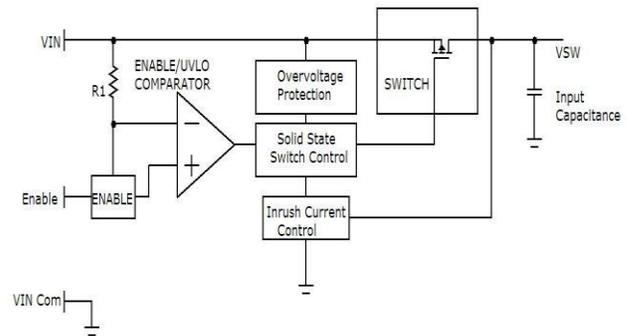
Figure 2: MFP Input Switch Functions

The SSS element shown in Figure 2 is a MOSFET. The default state for the SSS MOSFET is OFF. The switch is closed for input voltages between 3V and 6V while the unit is enabled. The SYNC pin can be used to monitor the state of the switch and is described in section 3.3. The addition of a series SSS greatly contributes to the MFP reliability and provides many additional features outlined in the following sections.

4.1.2 Input Bus Voltage Startup
The source for the bus feeding the POL is often a DC/DC converter whose behavior may pose reliability issues to the POL and its sensitive low-voltage load. These issues include non-monotonic startup, overshoot and undershoot and potentially result in Power-On Reset (POR) problems for digital loads. POL converters with narrow input ranges may aggravate upstream DC/DC converter power-up issues by creating output drop outs.

These issues can be solved by a POL with a wide ranging input that operates through typical source overshoot or undershoot events. Safe operation to 6V and greater on a 5V bus allows for source overshoot during startup or during line

and output load transients without damage to a wide-input converter such as the MFP. As a precaution and to allow for a controlled power-up, the SSS is not closed until the internal auxiliary power supply and internal control circuitry are fully functional.

4.2 Startup and Inrush Current Limiting

All POL converters require a large input capacitance for optimal performance. The capacitance is critical in order to meet stated load transient response and stability and to filter the large and discontinuous switching currents produced by POLs. A side effect of this large capacitance is a large inrush current upon application of power. This current, sometimes reaching values up to 100A, not only poses a risk to the input capacitor but also to upstream components. Inrush current limiting can be accomplished by adding a sensing resistance to the input along with control circuitry or by a simple series resistor. Both of these solutions negatively impact efficiency and the former increases circuit complexity.

Many first-stage converters may not be able to source or start up the large capacitances normally required with a POL and many are internally limited, entering hiccup mode or restarting when faced with such a large capacitance. Inrush current limiting within the MFP allows for predictable startup from bus sources that may be current-limited during downstream converter startup.

The MFP SSS shown in Figure 2 not only provides protection from input transients and misbehaving voltage sources but also allows a controlled startup. The MFP SSS operates as a linear regulator during startup, limiting the rate of change of the internal power bus to approximately 1 V per millisecond and in so doing provides inrush current limiting.

The MFP provides the input bus capacitance required to meet all of its specifications. This capacitance is connected to the internal power bus and is separated from the input bus voltage by the SSS. The inrush limiting through the SSS protects the large input capacitance used in the MFP from damage at startup to a safe level, improving reliability. The low and predictable inrush current can prevent a power-on reset event or non-monotonic startup from a current-limited or protected source.

For POLs that do not include the input bulk capacitance required for proper operation, sourcing the capacitor required can be problematic to the system designer due to the large inrush and ripple currents involved. The highest capacitance density technologies that would be favored in this application have reliability drawbacks. Qualification testing of the internal capacitors used in the MFP involved millions of startup cycles at extreme temperatures and significantly higher inrush currents than seen in actual application to provide the assurance of reliability.

4.3 Fault Detection and Propagation Prevention through Digital Diagnostics

While good design practices are the best fault prevention, it is still desirable to detect faults in complex power systems before collateral damage occurs. Faults at the inputs and outputs of POL devices, including over-current and over-voltage events should be monitored. Fault propagation prevention can mitigate damage by limiting the fault duration.

Although the interface to the MFP is purely analog, it provides the user with the ability to monitor performance and control many internal functions. The functions described below may be used to perform diagnostics and control specific functions of the MFP.

The MFP SSS status can be detected by the user via the SYNC pin. A logic "high" of >2.8V indicates the SSS is closed and is an "Input Power Good" indicator. A logic "low" voltage of < 0.8V on the pin indicates that the SSS is open. The SSS is open whenever the input voltage is below the under-voltage lockout, greater than the overvoltage shutdown, or the unit has been disabled.

The MFP SHARE pin can be used to determine the health of the MFP output and load. The output current magnitude can be determined by reading the analog SHARE pin voltage as illustrated in Figure 3.
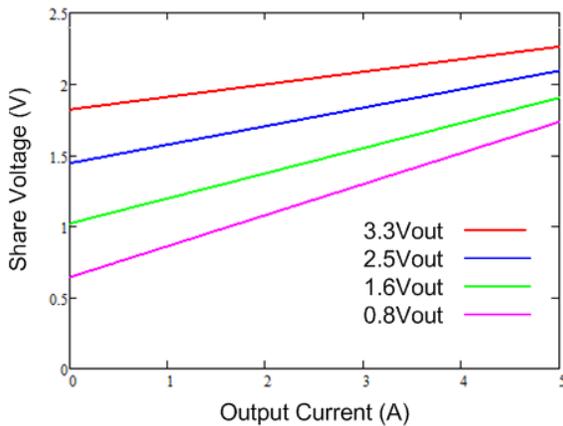
Figure 3: SHARE pin voltage as a function of output current at various output setpoints

The combined status of the SYNC and SHARE pin can be used to detect an output overvoltage or overload condition. A SHARE voltage in the expected range is an indication that the output voltage is present and properly regulating. An output overload or short will result in a SHARE pin voltage of 2.5V if the SSS is closed. A SHARE pin voltage less than 0.5V is an indication that the output is in an overvoltage condition if the SSS is closed. Table 1 shows the relationships between SHARE pin state, SYNC pin state, and fault condition. When a load or internal fault is detected via either of these monitoring methods, the ENABLE pin can be used to disconnect power from the load by

opening the SSS, allowing the user to implement external output overvoltage shutdown.

Table 1: Fault monitoring

SHARE state	SYNC state	Fault condition
< 0.5V	< 0.8V	Input < 2.0V
< 0.5V	> 2.8V	Output over-voltage
2.5V	>2.8V	Short / overload
0.5V – 2.5V	< 0.8V	Input Overvoltage
0.5V – 2.5V	> 2.8V	Normal operation, input voltage in range, output in regulation

4.4　Noise Considerations

A major area of concern, especially in noise-sensitive systems, is the amount of noise generated by switching power supplies. While most supplies switch in the hundreds of kHz, hard switching causes higher frequency harmonics to be introduced. These higher frequencies are then conducted through traces and radiated through the leads to other parts of the system. POL input and output filtering are essential for reducing noise to acceptable levels. These filters must be capable of handling frequencies in the tens of MHz.

The MFP includes a "pi" type input filter that greatly reduces the input current ripple noise and is particularly effective at reducing high frequency components. The low noise level of the MFP at high frequencies is particularly important in a system application. Higher frequencies can create significant problems with radiation from the leads.

Figure 4 is a spectral plot of the conducted emissions of the MFP with no additional external filtering. The test was performed to CE-03 of MIL-STD-461C. The plot indicates that the emissions at the 300kHz fundamental are 70dBuA or 3mA-RMS. The plot indicates that the noise level is extremely low for frequencies greater than 4MHz and illustrates the quiet operation of the MFP with no external filtering. The limit line in the plot is the maximum allowed vs. frequency for CE-03.
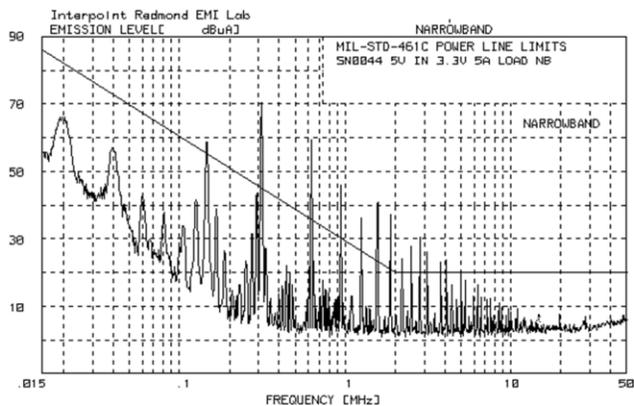
Figure 4: MFP Conducted Emissions, CE-03, Narrowband

Compliance with the limits of CE-03 is not often a requirement for a stand-alone POL but is usually a requirement for the system power applied to the input of the first stage converter.

Input ripple current can be seen in the time-domain images in Figure 5, Figure 6, and Figure 7. The bottom trace in each of these three oscilloscope figures shows the input ripple current measurement using three bandwidth limits of 10MHz, 20MHz and 200MHz, respectively. The plots of the MFP were taken with no external filter components and at full load. The behavior of the three figures at the increasing bandwidths and the lack of high frequency spikes are good indications of the effectiveness of the internal filtering. For the user, the predictable low-frequency input noise with the lack of high-frequency components makes the MFP easy to use in applications sensitive to noise.
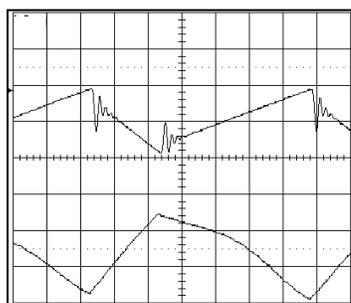
Figure 5: Output Ripple Voltage (Top, 20mV/Div), and Input Ripple Current (Bottom, 100mA/Div). Oscilloscope Bandwidth 20 Hz to 10 MHz
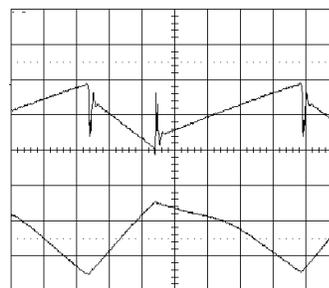
Figure 6: Output Ripple Voltage (Top, 20mV/Div), and Input Ripple Current (Bottom, 100mA/Div). Oscilloscope Bandwidth 20 Hz to 20 MHz
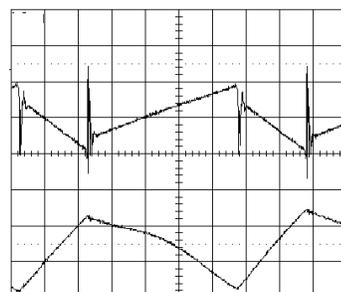
Figure 7: Output Ripple Voltage (Top, 20mV/Div), and Input Ripple Current (Bottom, 100mA/Div). Oscilloscope Bandwidth 20 Hz to 200 MHz

4.5 POL Switching Current Considerations

Low-voltage, high-power, POL devices create a large input RMS current proportional to the load current. Many available POL devices do not provide all of the input capacitance required to meet specified performance levels. In some cases the user is expected to design and supply the input capacitor with minimal information from the converter manufacturer, potentially resulting in serious reliability and stability issues.

In order to correctly specify the input capacitor, its type, capacitance, ESR, and ripple capability must be considered. The POL input current waveform with no input bulk capacitor is a square wave with a duty cycle equal to the ratio of the output voltage to the input voltage and a peak value equal to the POL output current. The maximum RMS current will occur when the duty cycle is 50% or when the output voltage is half

of the input voltage. The AC RMS input current can be calculated using Equation 1.

$$Icap_{RMS} := Io \cdot \sqrt{\left(1 - \frac{Vout}{Vin}\right)\frac{Vout}{Vin}}$$

Equation 1: Input RMS ripple current for a non-isolated POL as a function of output voltage, input voltage and output current.

For example, a POL with a 5V input, 3.3V output at 5A load, generates a RMS input ripple current equal to 2.4A.

If the user is providing all of the source capacitance and none is included internal to the POL then the user-supplied input capacitor must be rated (and appropriately de-rated) to handle this current. Equation 2 calculates the power dissipated in the source capacitance due to the input RMS ripple current. Many POL manufacturers do not quantify the reflected RMS ripple current produced, making capacitor derating more difficult. The user must then calculate the RMS ripple current and power dissipation, using both of these numbers to choose the right capacitor.

$$Pcap := Icap_{RMS}^{2} \cdot ESR$$

Equation 2: Power dissipation in the input capacitor is determined by the product of the RMS ripple current and the capacitor ESR (Equivalent Series Resistance)

The large, low-ESR capacitors needed to support a POL are subject to large inrush currents from the bus converter or source, affecting the types of capacitors that can be used. Aluminum electrolytic capacitors tolerate large inrush currents with relatively low ESR and high capacitance-voltage (CV) product; however the use of such components is often prohibited in high-reliability applications due to the catastrophic collateral damage that can result from component failure. Solid tantalum capacitors are the next best choice for input filtering, however these components do not tolerate large inrush currents by comparison and

thus require some degree of inrush limiting. The least desirable capacitor technology for input filtering is ceramic due to its low CV product.

The capacitance and ESR of the input capacitor can affect the performance of the POL in many ways not clearly visible to the end user. For example, the load transient response can be affected and the control loop stability margins can be inadvertently reduced. The wider the control loop bandwidth of the POL the more the source impedance, particularly the input capacitance, is reflected in the load transient response. The feedback loop stability of the POL can be negatively affected if the source impedance of the input network violates the Middlebrook criteria [5] of remaining less than the converter input impedance across the operating frequency range.

The impact to size, cost, and efficiency of a converter should an external capacitor be required needs to be considered when selecting a POL. The MFP eliminates concerns in a customer's application by addressing the design challenges and decisions required of the user. The required input capacitance is included inside the package and protection for the capacitor is provided by the internal SSS that mediates input transients, under and overvoltage protection and inrush current limiting. The bulk capacitance included in the MFP provides requisite margins for stability under all operating conditions and meets strict derating standards for voltage and RMS ripple current which have been fully tested and verified.

4.6 Output Voltage Set and Trim

POL converters available today commonly provide a single output voltage with limited trim, often +/-10%. This requires the user to purchase different POL converters for each output voltage needed. In some cases a wide-ranging output is provided but requires an external resistor to trim for a particular voltage. A large trim range, even with a precision resistor, may make accurate

voltage setting very difficult. The trim resistance required for a given output voltage may have an asymptotic relationship that limits the accuracy of trimming at the extremes of the trim range.

A single model of MFP POL has the flexibility to be set for any voltage from 0.64V to 3.5V. This product simplification allows the power system engineer to specify and qualify one device for many output voltage applications. The MFP includes five precision set-points that can be accomplished with pin connections alone and without an external trim resistor. The default output voltage with both pins open is a precise 0.8V +/-1.5%. Grounding one or the other or both of the two trim pins sets the output at an equally precise 1.6V, 2.5V or 3.3V. An additional precision preset of 0.64V will result from the connection of both trim pins to the positive sense pin. In-between values of output voltage can be set with the use of an external trim resistor in series with the trim pins to ground. The range between set points is small enough to make the selection of voltage by resistor more linear than products with wider trim ranges.

Having the ability to set the output voltage precisely by selectively grounding a two-pin combination also allows for easy digital control of the MFP in any one of the five preset voltages. Selecting output voltage under firmware or software control can have advantages where digital devices can be powered at different levels to trade off speed for power efficiency.

4.7 Output Noise and PARD
Output noise includes the periodic component synchronous with the switching frequency of the converter and random noise. Often referred to as PARD (Periodic and Random Deviation), the noise produced is one of the most problematic side effects of switch-mode converters. A POL may produce excessive high frequency noise for many reasons including synchronous rectification shoot through or delays, layout,

poorly designed output filter inductor, or higher-than-desired ESR in the output capacitor.

Some POL converters do not include the output filter capacitors while others include only a minimal amount and require additional external capacitance to meet their output noise specifications. If an output capacitor is to be selected by the user, the output RMS ripple current must be determined, and the proper rating for the capacitor selected, in order to ensure reliable operation. The output ripple current and dissipated power cannot be determined without knowledge of the output inductor design.

When a manufacturer specifies exactly how output ripple is to be measured or limits the bandwidth to a lower frequency, the user should be aware that the filtering provided may not be adequate for the user's application and that additional design measures may be required to use the product.

The MFP may be the quietest POL available today and achieves this without the use of any external capacitors or special measurement techniques. The output ripple and noise with three different bandwidth settings, 10MHz, 20MHz and 200MHz, are shown in Figure 5, Figure 6, and Figure 7. Comparing these three waveforms' amplitudes at increasing bandwidths demonstrates the lack of high frequency content. The MFP does not generate significant noise due in part to a novel cross conduction lockout circuit that maintains maximum conduction time but prevents shoot through under all load and environmental conditions. Additionally, the novel design of the output inductor minimizes noise, the surface layout traps noise, and the use of multiple technologies with staggered resonant frequencies in the output capacitance ensures better filter performance.

4.8 Load Transient Response
The response of a converter to a transient change in current is a transient change in output voltage.

An important consideration in the specification of a POL is the load transient response because many digital devices may have major internal transitions that result in rapid dynamic current demand while also requiring a tightly regulated supply voltage.

The instantaneous voltage change shown in Figure 8 in response to a load step is set by the ESR and ESL of the output capacitance as indicated by region 1. The rate at which the output voltage returns to the nominal value is dictated by the control loop response time and the value of the output capacitance. Region 2 includes the damped overshoot response.
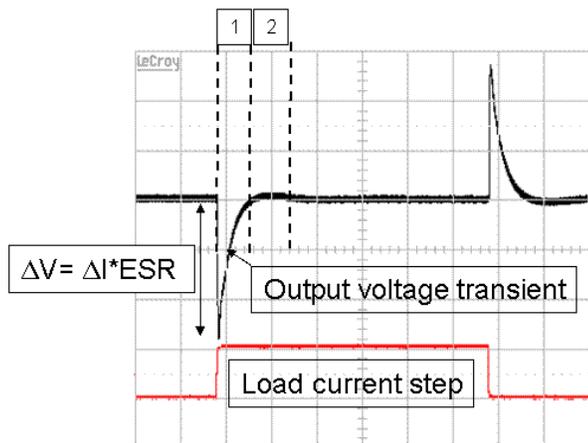
Figure 8: MFP 5Vin, 3.3Vout, half-load to full-load voltage transient (50mV/div vertical, 200us/div horizontal)

The rate of change of load current is not instantaneous and is important because the product of the rate and the Equivalent Series Inductance (ESL) of the output capacitance adds an additional voltage transient to the ESR-induced voltage step. The ESL-induced transient (not visible in Figure 8) is only present during the changing of the load current. The sudden load increase and resulting output voltage drop will continue to deplete the output capacitor until the POL control loop can increase the output current to meet the new demand.

Many POL products require some or all of the output capacitance to be added by the user external to the POL. This means that the magnitude of the load transient response and the selection of the appropriate capacitor types, sizes and ratings are up to the user. The user, in this case, must exercise care in the choice of capacitors with attention to ESR and ESL, in addition to optimizing the layout of the external components to minimize additional resistance and inductance which can increase the transient response.

The MFP simplifies the design challenge for the user because the component selection and layout decisions are already addressed internal to the device. All of the necessary output capacitance is included within the MFP package. The MFP includes significant capacitance chosen for low ESR and low ESL. Multiple capacitor technologies are used to ensure the lowest possible ESR and ESL over the widest frequency range. Figure 8 is the actual half-load-to-full-load transient response of the MFP. The undershoot is less than 150mV while the recovery time is short at approximately 160usec due to the wide bandwidth control loop. The lack of overshoot and critically damped response is due to the balance between stability and transient response.

The load transient response is affected by the loop gain, phase and bandwidth. The MFP uses a patent pending dual control loop approach to optimize the transient capabilities of the MFP. The dual loop is composed of an inner current loop and outer voltage loop. The general implementation is similar to a classic average current mode control. By utilizing a high bandwidth inner current control loop, the overall compensation can achieve wider bandwidth and greater design margins through the elimination of a pole in the voltage loop transfer function. The inner current loop is also an integral part of the current share and current limit circuitry and will be discussed in the following section.

```
A:T/R(dB)B: θ         ○ MKR          8 317.638 Hz
A MAX   50.00    dB    GAIN          26.8573   mdB
B MAX  225.0    deg  PHASE          85.6935     deg




A MIN  -50.00    dB    START          1 000.000 Hz
B MIN -225.0    deg    STOP         100 000.000 Hz
5VIN 3.3VOUT 5A    _
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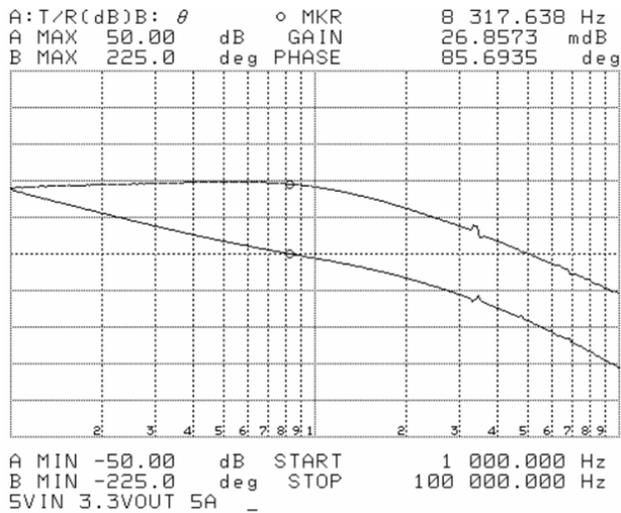
Figure 9: MFP Bode plot at 5Vin, 3.3Vout, full load

Figure 9 is an image of the gain-phase characteristics of the MFP. The image indicates the substantial phase and gain margins of 85 degrees and 19dB, respectively. The smooth gain rolloff of 6dB per decade is possible because of the nested current mode control loop and highlights the stability margin designed into the MFP.

This kind of control loop not only guarantees wide operating condition stability but also allows the addition of very large external capacitance without affecting the stability and performance of the MFP. The magnitude of the overshoot will decrease as capacitance is added assuming the ESR is low. The MFP is characterized and tested with an additional 5,000uF of capacitance to guarantee stability with large capacitive loads.

4.9   Current Limit and Current Share

4.9.1   Current Limit

Current limit protection is important in order to protect the POL from damage due to incidental overload or output shorts. It is crucial for system reliability to prevent the propagation of output faults back to the converter source or intermediate bus.

In order to prevent fault propagation, the overload or short circuit protection should be indefinite over the full operating temperature range; additionally, the short circuit fault should result in an input current to the POL equal to or less than the full load condition. The short circuit power dissipation should be specified so that the user can ensure that the maximum temperature of the POL is safe under short circuit conditions.

Many POLs use independent current limit circuits that become effective at an output current threshold and take control of the feedback from the voltage control loop. These current limit designs often result in unstable overload-to-short-circuit performance during the transition from voltage control to current control.

POL converters often use a current limiter that detects a fault and shuts off for a period of time, restarting automatically. This type of current limiter action is sometimes referred to as "hiccup mode". Although easy to implement, there are serious issues with this type of current limit control. Depending on the duration of the "hiccup" the POL may not be able to start large capacitive or complex loads because of the discharge of the output capacitance during the off time. For this reason, the peak current threshold for shutdown is often very high in hiccup-controlled converters, resulting in very high peak power transients. These types of limiters depend on a rate-controlled startup to avoid tripping the current limiter while the output capacitance is charging.

Some designs may use current fold-back to provide short circuit protection by reducing the output current as the output voltage declines. These designs often have difficulty starting complex loads and are best if the load is resistive. As such, they may not start a load with a constant current characteristic.

Some current limit designs are integrated with a peak current mode control IC. These cycle-by-cycle current limiters have a minimum duty cycle due to the propagation delay from detection of

overload to an OFF state on the power switch. This minimum duty cycle may result in a very high output current at a very low resistance short circuit. Higher operating frequencies result in increasing short circuit currents.

The MFP current limit protection circuitry is integrated into its feedback control loop. In current limit, the MFP smoothly transitions from a constant voltage mode of operation to a constant current mode. This type of current limit is desirable because of the stable operation provided independent of loading. The maximum current under short circuit conditions is constant independent of the POL frequency. The current limit is deliberately designed to exhibit a negative temperature coefficient to ensure reliable operation over the full operating temperature range. This means that the maximum current limit value occurs at the lowest temperature when power dissipation is least critical.

4.9.2 Current Sharing

Current sharing is a feature available on many converters, allowing multiple POL converters at the same output voltage to be used in parallel to drive larger loads. True current share between multiple converters requires some type of internal current mode control and a means of communicating the load current from one converter to another.

The simplest method of paralleling multiple converters is the connection of conventional voltage mode controlled devices in parallel. This is not an ideal method because the converters are not truly sharing the load current. Paralleling conventional voltage-controlled outputs results in the converter that has even a marginally higher output voltage carrying a majority of the load until overload occurs or until the output is pulled low enough for a second unit to support the load. In either case, the unbalanced loads among units in parallel result in significant stress with reliability consequences on the overloaded converter. A lower overall efficiency is a result of the imbalance because optimal efficiency will occur with identical loads.

Other methods of current share include a technique used first by Unitrode [4] allowing multiple units to operate in parallel by making a common share connection between converters. The method is based on a patented [2] internal circuit that elevates the voltage references of all converters to match the unit with the highest reference voltage. This technique works to balance loads but can result in an elevation of the output voltage of the paralleled converters. The external connections in this technique can be noise sensitive.

Other methods include designs that incorporate additional circuitry that can be accessed via a pin connection to allow one converter to operate as a master and a second as a current slave. The signal is usually a voltage or current proportional to the load current. This method may require multiple pin connections and the designation of a unit as a master or slave.

The MFP POL is capable of current sharing with up to five units in parallel and uses a method similar to the method described in the previous paragraph. Additional units can be safely shared with a resulting drop in the maximum power available from each. As mentioned earlier, the MFP includes an inner current control loop. A single external SHARE pin allows access to the interface between the outer voltage control loop and the inner current control loop. Connecting this pin between multiple MFP converters will allow accurate current share between multiple units driving a common load.

When multiple MFP converters are connected in parallel to a common load, the output voltage should be set by a single converter selected by the user as the "master." All units except for the master should have their output voltage set pins connected to the positive output while the master

can be set for any voltage using the two preset pins and trim resistors as required. The voltage setpoint can be changed real-time as needed on a single unit.
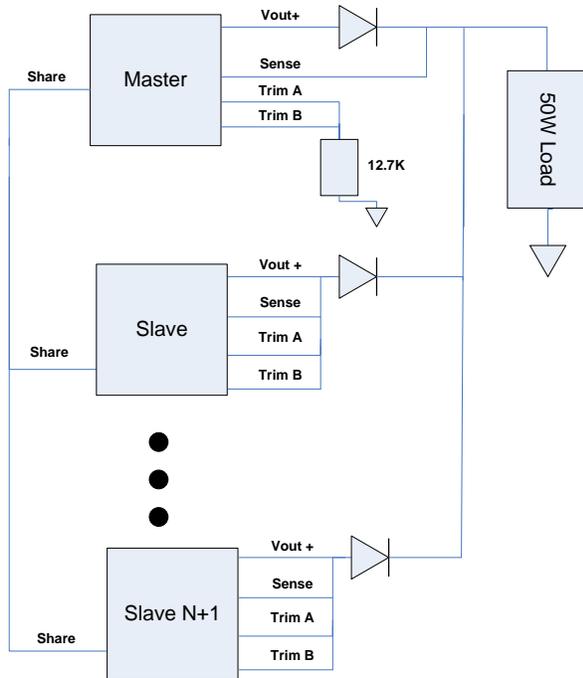
Figure 10: Current sharing connection including N+1 redundancy

Because of the MFP's inner current loop, voltage loop gain and phase characteristics are constant and are independent of the number of units in parallel. The minimum gain and phase margins including the use of large capacitive loads are guaranteed. Short circuit performance and freedom from large overshoots under a variety of load conditions are among the benefits of the topology utilized in the MFP.

Current share accuracy of the MFP is very precise because the voltage present on the current share pin of each converter is a highly accurate measure of the load current.

It is possible with this method of current share to implement an "N+1"architecture with the use of external low-Vf Schottky diodes, as shown in Figure 10. The Schottky diodes serve to isolate a

faulty POL converter from the load, allowing it to drop out without consequence to the load. For true "N+1" redundancy, at least two of the converters in parallel should have the trim pins set for the same output voltage. If an output voltage change is required in circuit, both units would need to be changed.

4.10 Synchronization

Synchronization can be a very useful feature because it affords the user flexibility when managing noise. When synchronized, the power conversion frequency of the POL can match that of other sources in the power system for ease of filtering. Multiple power converters operating at different frequencies may interfere with one another, resulting in higher input and output noise. In such a system, it is possible to generate conducted audio noise resulting from "beat frequencies" that are the difference between clock signals of different converters. The low-frequency "beats" are difficult to filter in the audio range and may create problems for systems that require low analog signal noise.

Another very important reason to synchronize in a digital system is the ability to predict the timing for noise spikes and to clock digital devices or A/D and D/A devices at a synch frequency multiple. This timing prediction can be used to desensitize the system to converter noise by sampling or converting in the "quiet" period between clock transitions.

The MFP is one of very few POL converters provided with a synchronization feature. The MFP can synchronize over a wide frequency range up to 600 kHz. This feature allows maximum flexibility for integration with a system clock and with other switching converters. The nominal switching frequency of the synchronization signal is often generated as a system clock that may be common with, or a multiple of, the system processor or other digital devices. The nominal switching frequency of the MFP is 300 KHz, +/-30 KHz. Efficiency is

slightly reduced due to switching losses at sync frequencies above 330kHz, as shown in Figure 11.

4.11 Enable/Inhibit and Sequencing

Most POL devices include a method of disabling power conversion. This function is useful to shut the POL off when not needed, reducing power consumption. Some POL devices include a tracking feature, allowing multiple devices from a single manufacturer to start with a proportional voltage to a given output. An Inhibit or Enable feature is useful in timing multiple units during startup, enabling certain voltages to be up before others. Multiple MFP devices using common ENABLE timing will track during start-up.

The ENABLE function in the MFP is a TTL-compatible input with a 1.8V threshold. A "logic low" on this pin will result in no output voltage and a low quiescent current. The action of the ENABLE circuit is to open the internal SSS, disconnecting the input from the power train. The MFP internal supply will continue to operate during disabled operation to ensure that ENABLE logic levels are maintained and to ensure a rapid and controlled startup with the ENABLE action. A voltage on the pin greater than the ENABLE threshold or an open circuit closes the internal SSS and allows for normal POL operation.

The precision of the ENABLE threshold allows this pin to be used to precisely set a startup delay with the use of a capacitor on the ENABLE pin. Diodes can be used on the ENABLE pins to isolate each POL converter and individual capacitors can be used to adjust startup delays for each unit from a single master ENABLE command.

4.12 Efficiency

Efficiency is one of the more important parameters in selecting a non-isolated POL and is the percentage of power delivered from the converter to the total power input to the converter, as shown in Equation 3.

$$\eta = \frac{Pout}{Pout + Ploss}$$

η	defined as Efficiency
Pout	defined as output power
Ploss	defined as internal power loss

Equation 3: Efficiency

Efficiency varies with input and output voltage, load and temperature. High efficiency power conversion is important for two major reasons. First and foremost it is critical in battery powered applications in order to minimize total power loss and extend battery life. Second, high efficiency minimizes POL self-heating and the associated heat-sinking requirements.

Power loss in a POL converter falls into three broad categories. The first category is internal control and gate drive losses. These losses are fixed and are independent of the POL loading. The second type of loss is transition losses of the power MOSFETS. These losses occur during the switching of the high current power train and are proportional to load current. The third type of loss is powertrain conduction losses that increase as the square of the load current. Conduction losses also increase with temperature as the resistances of various conductor materials increase. The shape of the efficiency curve indicates the significance of these individual effects.

Decreases in light load efficiency are due to the proportion of fixed control losses increasing as total power is decreasing. This effect can be pronounced at lower output voltages where the total power delivered is at a minimum.

The roll off of efficiency at large output load currents is due to the second order losses of conduction. If full load efficiency roll-off is not present, then the manufacturer has limited

maximum power to a level where conduction losses are not dominant at full load but are still roughly equivalent to control losses. If significant roll off at full load is present at room temperature then the efficiency drop at high temperatures will be even more pronounced because conduction losses increase as temperature increases by roughly 40% per 100 $^{\circ}$C. Efficiency and power dissipation should be considered at the maximum output power where the device is used rather than at an intermediate point where the efficiency may be highest.

Feature rich POL converters which offer synchronization such as the MFP introduce further consideration when determining how one wishes to configure the power system. General switch losses are composed of a number of factors, including gate charge loss from driving the MOSFETS, switching loss from non-ideal voltage-current transitions, and conduction loss. Illustrated in Figure 11 is an example of the contribution of each MOSFET loss term as a function of frequency. The highlight of this plot is the overall converter efficiency as the synchronization frequency is increased from 200 kHz to 1 MHz, at full load. In this example, from 400 kHz on gate charge loss becomes the dominant factor, while switching loss maintains a similarly large contribution and conduction loss holds relatively constant for a given load.
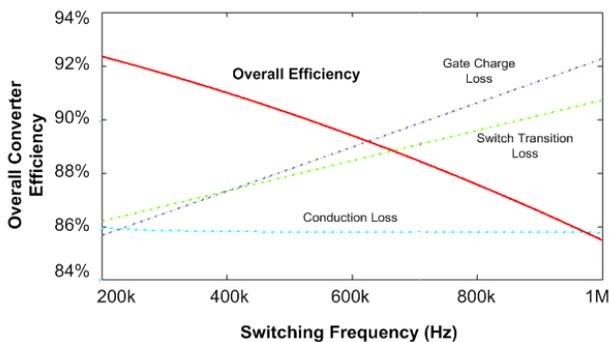
Figure 11: MFP switch loss and converter efficiency vs. frequency

While higher frequency conversion allows for reduced converter footprints because of smaller

magnetics, the MOSFET characteristics greatly influence the optimal switching frequency when considering the point of greatest efficiency. And while synchronization features allow frequencies over twice the free-run frequency of some POL converters, optimum efficiency will often be found with frequencies closer to the free-run frequency of the converter as originally designed. Still, in this example the MFP shows great versatility with relatively minimal increased loss and full operation capability over an impressively wide frequency range.

Another consideration for many POL converters that use synchronous MOSFETs is that they can have a more significant light-load efficiency roll off than non-synchronous designs due only to control losses. Inherent to all Buck converters is a transition from a continuous to a discontinuous mode of operation at light loads. When the converter is implemented with a low-side diode, the output conduction is cut-off at light-load creating discontinuous conduction. When synchronous MOSFETs are used for rectification, conduction is not cut-off at light loads but instead a large recirculating secondary current is created in the reverse direction. This current results in a resistive loss from what is effectively internal loading of the POL as it discharges the output capacitance back through the powertrain, as shown in Figure 12. This light-load recirculating current results in reduced efficiency because of the resistances in the power train and the losses incurred from the input and output non-ideal reactive components passing energy back and forth. Depending on the design, the discontinuous current can occur at loads as high as 50% of full load. Different POL converters vary in the level of sophistication used to manage this problem.
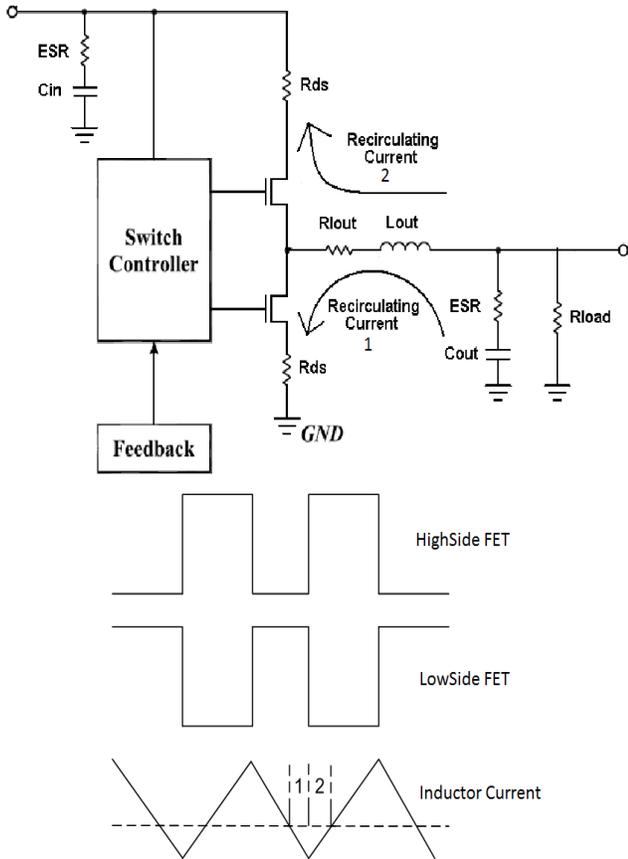
Figure 12: Synchronous MOSFET recirculating current

Some designs stop the synchronous MOSFET rectification at light loads above the discontinuous current and allow MOSFET body-drain diodes to manage rectification. While power dissipation is reduced in this scheme, it is not optimal due to the use of a junction that was not designed for rectification. In addition, the transition from synchronous to conventional rectification can cause an output voltage transient as the synchronous output shuts off. Operation near this transition may result in oscillatory behavior.

Some sophisticated designs detect the onset of discontinuity, shutting the synchronous MOSFET off at exactly the right time cycle by cycle. This duty cycle modulation allows the converter to become discontinuous but requires very accurate detection and MOSFET gate timing. The operation of a converter in the discontinuous region degrades load transient response due to reduced control loop bandwidth.

The MFP took a new approach to solve this problem with a proprietary technology embodied within a unique circuit. The design enables the converter to maintain forward continuous conduction operation down to very light load conditions with minimal recirculating current. There is no abrupt transition from synchronous to conventional rectification or dramatically reduced bandwidth since continuous condition is maintained.

Figure 13 shows the efficiency of the MFP at three different output voltages. At the lower output voltages, efficiency is reduced because of to the lower output power yet constant overhead losses. While efficiency remains flat to the full rated load at the higher output voltages, full load efficiency drops very slightly at the lowest output voltage as conduction losses become more significant.
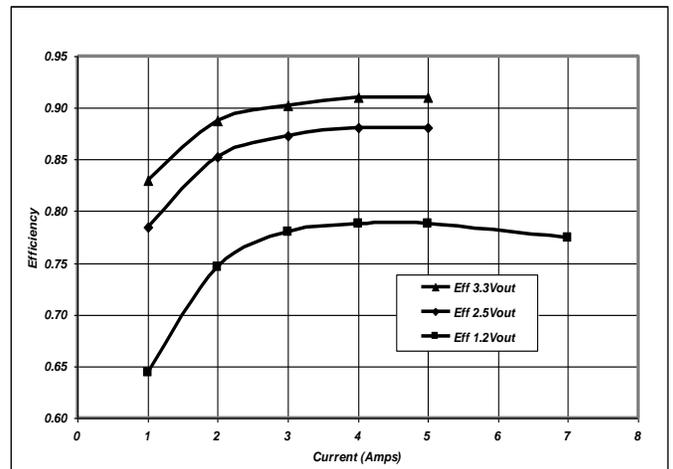
Figure 12: Typical MFP efficiency vs. load

5 Environmental Design Considerations

5.1 Product Performance in Harsh Environments

Many POL devices are available at high power densities and with a high degree of functionality.

The majority of assembly and packaging technologies employed are suited to the highest volume applications in computing and communications while few technologies are suited to operate in harsh thermal and mechanical environments.

The MFP is constructed using hermetic hybrid construction for the ultimate in environmental ruggedness and reliability. Interpoint brand products are among very few available as hybrid microcircuits, using bare die attachment,, wire bonded and sealed in a hermetic metal package backfilled with Nitrogen. Hybrid package technology allows control of all aspects of component interconnection and bonding, enabling the product to tolerate environmental extremes far beyond any other packaging technology. The MFP handles processing temperatures from below -70^{o}C to greater than 150^{o}C, sustains acceleration loads in excess of 5,000Gs, withstands random vibration greater than 45GRMS, and tolerates hundreds of high-rate temperature cycles from -65^{o}C to 150^{o}C. The MFP can operate indefinitely in a vacuum or at pressures of more than four Atmospheres. Because of the hermetic package, the product is not susceptible to solvents, cleaning agents, or contaminants. The steel package is plated with a Nickel finish and meets the highest ASTM and DOD standards.

The MFP's construction, processes and process controls are identical no matter what screening level is chosen. Interpoint products are among few hybrid microcircuits manufactured and fully qualified to MIL-PRF-38534 Class H and Class K.

5.2 Thermal Management

An advantage of a hybrid metal package is its superior thermal management with predictable and low thermal rise of all internal components. All die and magnetics are attached to a 96.5% Alumina, high thermal conductivity substrate. The substrate in turn is bonded to the steel package. This construction provides the internal components with the lowest practical thermal resistance from component hotspot to the base of the steel package, minimizing thermal rise. The large steel base provides an isothermic surface for mounting with the low thermal resistance and thickness of the steel creating significant heat-spreading.

As a result of the MFP construction, conservative design practices and high efficiency, all die hotspots are typically within 6 ^{o}C of the base of the metal package when operated at full load. Figure 13 is a thermal image of an open MFP operating at full load. The base of the MFP package is the preferred heat sink surface. All operating temperature references are with respect to this metal surface.
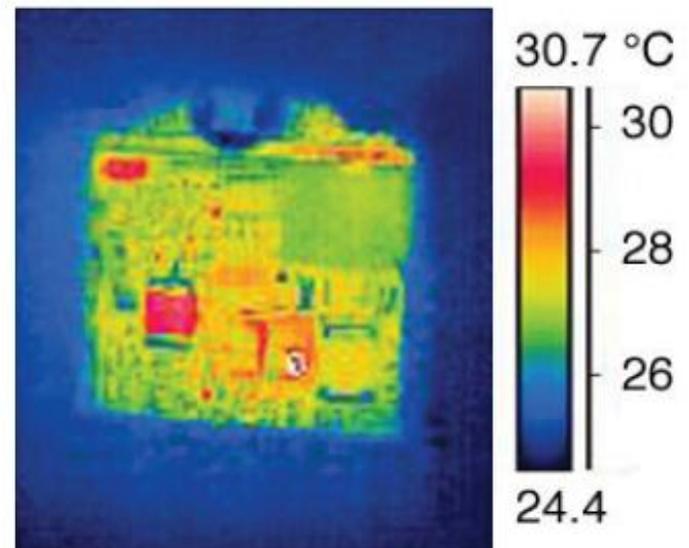
Figure 13: Thermal image of the MFP at 6Vin, 3.3Vout and 5Amp load. Base of the package at 24 ^{o}C. Maximum hot spot temperature is 30.7 ^{o}C.

5.3 Product Usability

"Product usability" refers to the practical application of the product. For a product to be usable, its power dissipation must be low enough to allow mounting and operation at the maximum load without concerns about the product's operating temperature and potential heating of adjacent components. A POL converter must be

able to be mounted close to the load without extreme measures for cooling such as heat sinks, moving air, or conductive metal mounting. If extreme measures are required to provide adequate cooling, the ability to mount close to the point of use is compromised and the overall footprint negatively impacted.

The thermal rise of a convectively-cooled POL mounted on a circuit card is proportional to the surface area of the product and the internal dissipation. The internal dissipation can be calculated from the output power and efficiency as indicated in Equation 3. If a POL product is rated at too high a power for a given package size or area, the product may not be usable in many applications without increasing mount area or volume via heat-sinking. The user should be cautious when using power density as a figure of merit in the selection of a POL because the product may not be usable at full rated power and the efficiency may be much lower than anticipated due to elevated operating temperature.

The Interpoint MFP dissipates $1W/in^2$ or less at its maximum output power. At lower output voltages and full rated load, the dissipation is only $0.5W/in^2$. The low dissipated power per square inch of surface area makes the MFP very usable for surface mount applications using only still air convection cooling. In any application, lower dissipated power density means lower device temperatures and thus higher allowed ambient air temperatures. The payoff is long term reliability due to lower operating temperatures. The MFP's excellent thermal management attained through hybrid construction coupled with conservative internal design results in reduced case temperatures and makes the MFP a very usable and practical POL.

5.4 Vibration

Vibration is another frequent requirement for use in harsh environments. By using a spectrum of vibration frequencies for testing, mechanical resonances inherent to the type of construction can be uncovered and investigated to ensure reliability. Random vibration is a more effective screen than other methods including swept sine wave methods. Random vibration is a realistic condition in which all frequencies are present because system nonlinearities may create modes not present in single frequency excitation. Few manufacturers address random vibration analysis and qualification. When designing a discrete POL, or one requiring large external components, the user must employ extensive mechanical analysis and testing to avoid shock and vibration issues during qualification.

The MFP has been subjected to Random Vibration tests as a part of product qualification using Method 2026 of MIL-STD-883. This method includes higher levels of vibration over a wider frequency range than other common methods in MIL-STD-202 or MIL-STD-810, as it was drafted for low-mass microcircuits. The MFP was tested at the highest level in Method 2026, 51.1GRMS, and for the longest duration, 15 minutes in each axis. Figure 15 and Figure 15 are excerpts from Method 2026 showing the spectra and conditions. The MFPs mounted prior to vibration testing can be seen in Figure 16. Results of the vibration testing are included in Figure 17. All qualification units successfully passed the testing.
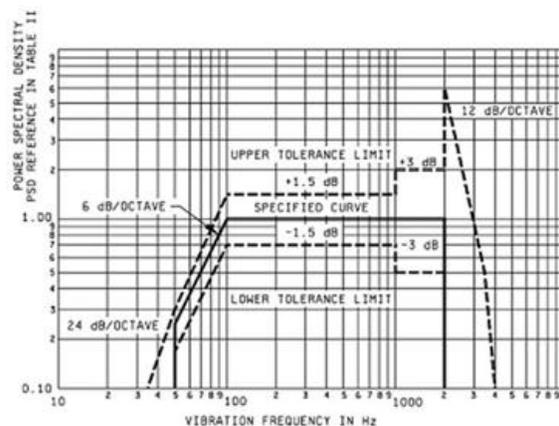
Figure 14: Excerpt from Method 2026 of MIL-STD-883. Random vibration spectrum.

Characteristics		
Test condition letter	Power spectral density	Overall rms G
A	.02	5.2
B	.04	7.3
C	.06	9.0
D	.1	11.6
E	.2	16.4
F	.3	20.0
G	.4	23.1
H	.6	28.4
J	1.0	36.6
K	1.5	44.8

Figure 15: Excerpt from Method 2026 of MIL-STD-883. Random vibration conditions.
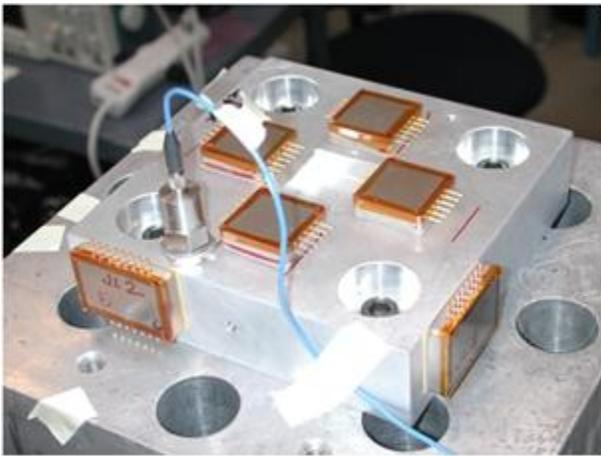
Figure 16: MFP units mounted on the shaker table for random vibration testing

.
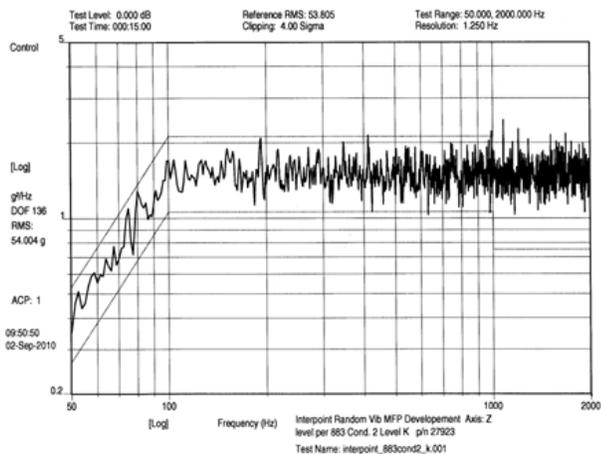
Figure 17: Acceleration sensor plot showing actual spectral levels during vibration testing of the MFP to level K.

5.5 Product Design Analysis

The design of a high reliability power converter should be supported at a minimum by the following analyses:

- Worst Case Analysis
- Electrical Stress Analysis
- Thermal Stress Analysis
- Derating Analysis
- Mean Time Between Failure
- Failure Modes and Effects Analysis

These basic analyses are important to ensure that the product will meet all specifications before and after leaving the manufacturing facility and will operate reliably in the customer application.

5.5.1 Worst Case Analysis

A Worst Case Analysis (WCA) is a critically important analysis in that it can detect marginal designs which may result in failure with component variation and drift or when operating under extreme conditions. WCA techniques from least conservative to most conservative are Monte Carlo, Root Sum Squares (RSS), and Extreme Value Analysis (EVA). A Monte Carlo analysis uses repeated random sampling to determine the likelihood of a failure mechanism. Although useful for sensitivity analyses, this analysis type does not contain the amount of rigor necessary to highlight specific, marginal design conditions. RSS analysis assumes that the likelihood of all worst case conditions occurring at the same time is small and assumes circuit variability follows a normal distribution. While information regarding likelihood of failure can be derived, absolute extreme case margin is not defined. Interpoint products use the EVA approach, where the combination of the most extreme component variation and operating conditions are determined for each individual component and performance parameter to determine absolute worst case design margins. This method is very conservative, but results in the greatest design margin and the highest reliability.

5.5.2 Stress Analysis and Derating

Stress and derating analyses compute the worst case electrical and thermal component stresses and compare those values to the maximum allowed manufacturer ratings. Derating is often applied to limit maximum component stress to a percentage of the manufacturer's rating.

The least desirable method for stress analysis is the "build and measure" technique, employing no analytical rigor. When an analysis is performed, the inputs may be either nominal or worst case. Values derived from simulation are usually nominal while extreme-value-based stress analysis uses the worst case operating conditions and worst case component parameters to calculate the component stress. The quality of the electrical stress analysis used for derating will ultimately affect the reliability of the product.

Derating, when applied, can enhance the reliability and improve the longevity of the product by operating components at a fraction of their rating. Derating standards among manufacturers vary from none at all to significant derating, the latter being employed where high reliability is demonstrated.

The Interpoint analysis method shown in Figure 18 starts with an EVA WCA whose outputs are used as inputs into the worst case Electrical and Thermal Stress Analysis (ETSA). The worst case electrical stress results are in turn used to calculate component derating and worst case thermal stress. The thermal analysis uses the worst case thermal resistance, component sizes and power dissipation combined with a conduction-only model to arrive at the worst case thermal rise. Thermal imaging is used as a validation of the analytical approach. Relying on thermal imaging alone is not a robust technique because it does not account for worst case component values, operating conditions or construction.
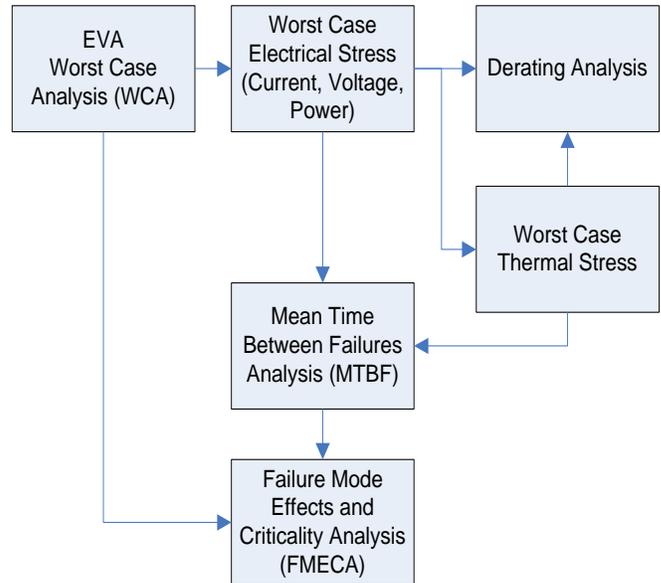
Figure 18: Crane Electronics Inc. Analysis Method

Derating based on nominal operating conditions and component values does not ensure worst case margin. Interpoint products employ the worst case electrical and thermal stresses to arrive at a derating analysis using a strict, proprietary derating standard based on MIL-STD-975M and MIL-STD-1547. Component derating is a cornerstone of reliable operation and should take into account the worst possible combination of component value and environmental, line, and load conditions for the converter.

5.5.3 Mean Time Between Failures Analysis

The derating analyses outputs feed into the final analytical indicator of reliability, the MTBF analysis. Interpoint products' MTBF analyses are performed to MIL-HDBK-217F with some modifications. Later revisions of this drawing do not require the inclusion of magnetic components and resistors based on the assumption that these do not contribute significantly to failure rate. Interpoint products are analyzed using a modified standard because, particularly in the case of a DC/DC converter, these components do impact reliability.

Interpoint products' MTBF are calculated by using the worst case component hot-spot

temperature and electrical stress as calculated in the ETSA. Although not required, all passive devices are included in the calculation. The calculation is made for all environmental conditions over a wide range of temperatures. The plotted results from the MFP analysis can be seen in Figure 19 and Figure 20. The conditions for the MTBF include the benign conditions of Ground Benign (GB) and Space Flight (SF), to the more severe Missile Launch (ML) and Cruise Missile Launch (CL).
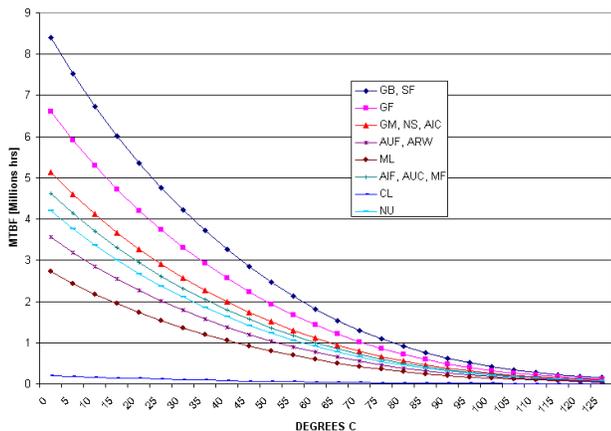
Figure 19: MTBF calculated for the MFP per MIL-HDBK-217F including magnetics and resistors for all conditions from 0C to 125C
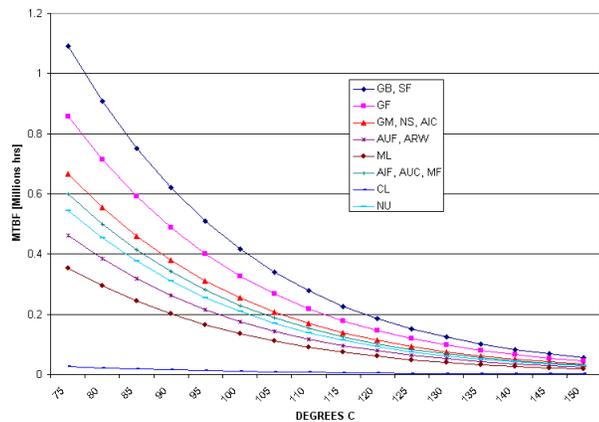
Figure 20: MTBF calculated for the MFP per per MIL-HDBK-217F including magnetics and resistors for all conditions from 75C to 150C

5.6   Screening and Radiation

There is a varying level of Radiation Hardness Assurance (RHA) for POL devices currently available. Not all manufacturers offer devices at every performance level. At a given radiation tolerance level, the analysis, qualification, and ongoing screening undertaken to claim such performance are not consistent across manufacturers.

The MFP is available in a range of screening offerings from unscreened industrial products to MIL-PRF-38534 Class K. Such certification is a comprehensive government-managed program audited to the strictest standards covering every aspect of manufacturing and product assurance. Radiation tolerant devices are available with guarantees to Total Ionizing Dose (TID) at levels of 30 and 100KRad(Si) in compliance with MIL-PRF-38534 through a Defense Logistics Agency (DLA, previously DSCC) approved RHA program. Interpoint products are among very few guaranteed with such an approved RHA plan.

The qualification process to complete RHA includes the completion of an EVA using post radiation limits from the Source Control Drawings (SCD). All integrated circuits and many semiconductors are lot-tested to the limits in the component SCD prior to acceptance. Every wafer of every wafer lot used is tested. Initial qualification, major change qualification and periodic testing are performed at 150% of guaranteed TID.

The Interpoint RHA program has several key components. The foundation of RHA is a worst case analysis based on EVA methods. The worst-case component assumptions used in the EVA WCA are in turn used to drive the lot- and wafer-based acceptance of components used to build guaranteed products. End item qualification testing occurs in parallel with the analysis and the associated restrictions placed on radiation-sensitive components. As a final check for the design and analysis, the end item is tested beyond the guaranteed TID to a level of at least 150% TID. These tests are performed both biased and unbiased to ensure that the worst-case condition is tested.

Historical testing for TID has been performed at very high dose rates. More recently, testing is also performed at very low dose rates representative of an actual application. Testing at low dose rate has been shown to cause failures not found at high dose rates. The MFP has been tested at both high and low dose rates to expose Enhanced Low Dose Rate Sensitivity (ELDRS) effects. The MFP meets its specifications to full intended dose.

Interpoint products include testing and guarantees of Single Event Effects (SEE) performance. The MFP has demonstrated survival and no latch with Linear Energy Transfer (LET) levels of 82 MeV-cm^2/mg. Radiation performance data is available upon request and may be subject to license restrictions.

6 MFP Product Summary

Today's system designers are faced with numerous challenges when selecting the correct powering solution for their sensitive, low voltage loads. Some of the most common and consistently difficult challenges are:

- The voltages needed to power the point of use are both diverse and precise while the bus voltages available upstream are not always regulated or well-behaved.
- Supply chain simplification is driving a reduction in the number of product variants desired to power each load.
- Most POL devices require external components for filtering and inrush limiting with little guidance about reliable component selection for such tasks. Such external components are not included in cost, efficiency, size, and reliability specifications and add extra time and work to implement.
- System-level noise requirements are quite stringent and are difficult to meet when each component is operating on a separate clock.
- The increasingly reduced size of power devices is achieved at the expense of usability, requiring more elaborate and expensive means of heat removal.
- Environmental and operating guarantees, ranging from component derating to radiation performance, can be achieved in a variety of ways with different levels of rigor.

The MFP Series™ products were specifically developed to address each issue above, making the selection, design-in, maintenance, and use hassle-free.

For further information, visit www.craneae.com/interpoint to download the MFP datasheet or to contact Crane Aerospace & Electronics for application inquires.

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